An Energy Efficient Design of High-Speed Ternary CAM Using Match-Line Segmentation and Resistive Feedback in Sense Amplifier

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Abstract— **This paper presents a high-speed and low-energy match line (ML) sensing scheme for ternary content addressable memory (TCAM). The proposed sensing scheme employs selective precharge which performs partial comparison on the TCAM words to eliminate most of the mismatched words from further comparison. Use of positive feedback in the sense amplifiers engaged in this phase speeds up search operation and reduces energy consumption. In the next phase, remaining portions of those words which were matched in the first phase are scanned to find the fully matched words. Lower resistance in the charging path of the sense amplifier in the second phase causes fast match detection. The proposed technique is simulated using 130nm 1.2V CMOS logic. Compared to conventional current-race (CR) sensing scheme the proposed scheme shows 26.5% speed enhancement and at least 31% energy reduction at the cost of insignificant area overhead and small voltage margin degradation. Unlike many CR type schemes, no analog control voltage has been used in the proposed scheme.**

Index Terms— **content-addressable memory, energy consumption, feedback, selective precharge, sense amplifier, sensing scheme, ternary**

I. INTRODUCTION

Present internet protocol (IP) packet forwarding and classification performed in network routers and switches require high speed search capability to decide which action to be taken on the packet. Routers extract the information (such as destination address) contained in the packet header and search a table called routing table to find the most suitable match. Though software based search techniques are available, these are inherently slow as several instructions need to be executed and multiple memory accesses to external RAM are required to find a match [1]. Ternary content-addressable memory (TCAM) offers a high speed hardware solution to this problem [2]. TCAM can compare an input search data against a table of stored data and can return the address of the matching data in a single cycle. It can store don't care values which may result in multiple matches. The most suitable match is selected by a priority encoder. This makes TCAM even more attractive for network applications because of the requirement of finding the longest prefix match i.e. match with the entry having the fewest don't care values.

A conventional TCAM cell contains two SRAM cells and comparison logic as shown in Fig. 1a. Both NAND and NOR versions of comparison logic are popular. But the NOR type comparison logic, shown in Fig. 1a, has some advantages over NAND type and hence is more prevalent [2]. The stored data (Data1Data2) is coded to represent three states such as '0' (01), '1' (10) and don't care or 'X' (00). Don't care bits always result in match irrespective of search data bits. Search data (SL1SL2) is provided through search line (SL) pair. In case of a mismatch the match line (ML) is pulled down to ground through one of the paths M1M2 or M3M4. Otherwise there is no connection between ML and ground. Multiple cells having a common ML form a TCAM word. And a TCAM array contains a number of such words as shown in Fig. 1b. One pair of SLs is shared by all cells in a column. A major disadvantage of TCAM is high energy consumption resulting from frequent switching of highly capacitive MLs and SLs. Reducing energy consumption remains a major challenge for TCAM designers.

II. PREVIOUS WORK

In the conventional TCAM the MLs are precharged to high and the SLs are precharged to ground [3]. Then search data is supplied. If there is a match between the search data and the stored data there is no conduction path from ML to ground and ML voltage remains high. If there is even a single mismatch, the ML voltage discharges to 0 through comparison logic in the mismatched TCAM cell. The match line sense amplifier (MLSA) outputs low at MLSO for mismatched MLs. Since only a few MLs are matched in a search, a large
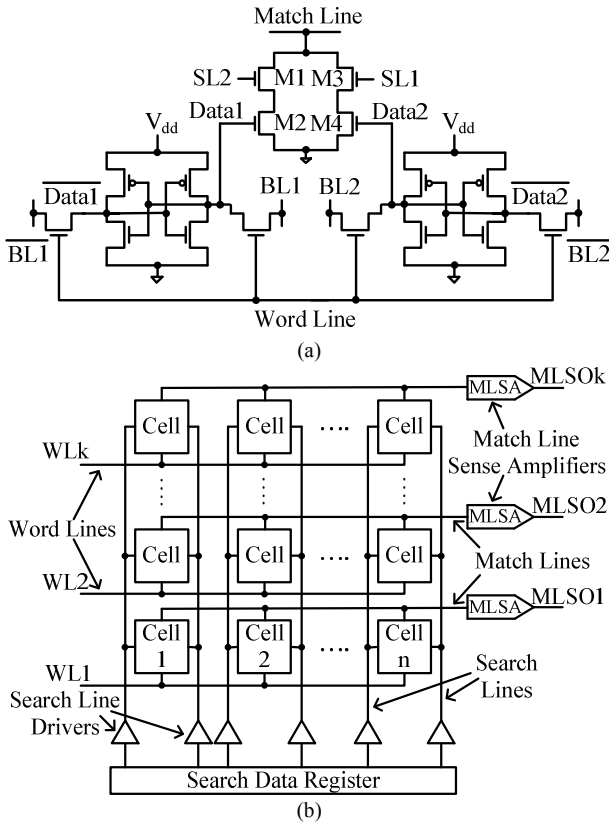
Figure 1. (a) A conventional TCAM cell consisting of two SRAM cells and NOR-type comparison logic. (b) Block diagram of a simplified k-word × n-bit TCAM array. Bit lines (BLs) have not been shown.

amount of energy is wasted in charging large number of MLs in the array.

A number of techniques have been proposed to reduce the energy consumption. Some schemes are selective precharge/pipelining scheme [4]-[5], pre-computation based scheme [6], bank selection scheme [7], block encoding scheme [8], charge sharing techniques [9]-[12] and current race technique with/without feedback [13]-[15]. Selective precharge/pipelining scheme divides ML into two (selective precharge) or more (pipelining) segments and perform comparison serially segment by segment. Only if the current segment being compared fully matches with the search data fragment then the next segment is activated and compared. The effectiveness of this technique depends on the distribution of the data and in the worst case there is no energy saving at all. Before the actual search operation begins, pre-computation based scheme performs some initial search to determine which MLs need to be activated for comparison. For example, the initial search may compare total number of ones present in a stored word and the search word. This technique requires additional circuits and evaluation time to perform the initial search. Bank selection scheme divides all the words into subsets called banks. During the search only the relevant bank in activated and compared. The problem with this technique is bank overflow which happens when the number of input combinations exceeds the storage capacity of a bank. Block encoding scheme uses some special encoding to compress IP addresses and thus reduces number of words

needed to be stored. Energy reduction is achieved by reduction of TCAM array size. Charge sharing techniques use either a separate capacitor [9], [10] or segment(s) of the ML [11], [12] to store charge in the precharge or partial comparison phase, respectively. This charge is shared with the ML or remaining ML segment(s) in the next phase. Techniques in [9], [10] are often referred to as low swing schemes as they reduce the ML power by reducing the ML swing voltage. But they suffer from the problem of low noise margin and area penalty arising from the extra capacitor. The technique in [11] uses complex match sensor block which requires additional control signals for its operation. The technique in [12] achieves small performance enhancement in terms of both search speed and energy consumption at the cost of significant implementation complexity. In current race (CR) technique [13], shown in Fig. 2, the MLs are pre-discharged to ground and during the search they are charged towards high. SLs need not to be pre-discharged to ground in this technique. This reduced SL switching activity compared to the conventional scheme saves energy. For fully matched words the corresponding MLs get quickly charged to a threshold which causes the sensing unit to output high. For mismatched words, MLs have discharging paths to ground and hence cannot be charged up to that threshold. So, outputs of the associated MLSAs remain low. A dummy word resembling a fully matched word is used to control the charging duration of MLs. During the charging phase CR scheme supplies the same currents to both matched and mismatched MLs. So, here also large amount of energy is wasted in large number of mismatched MLs. Feedback in MLSA has been used to reduce the current to the mismatched MLs in
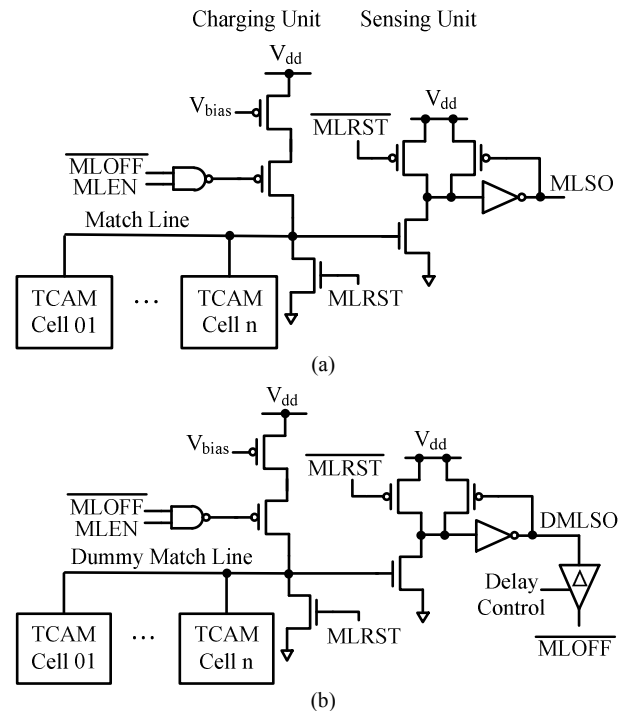

Figure 2. Current-race sensing scheme - (a) one TCAM word with MLSA consisting of charging unit and sensing unit and (b) a dummy word resembling an always-matched word.

[14], [15]. The mismatch dependant (MD) MLSA in [14] suffers from the problem that, when idle, there is a dc path from V_{dd} to ground causing static power consumption. The active feedback (AF) MLSA in [15] overcomes this problem by redesigning the charging unit. The techniques in [13]-[15] require additional control signals (such as V_{bias} used in [14] to offset the effect of process variation). These signals have to be generated on-chip or have to be supplied off-chip.

In this paper we propose a ML sensing scheme where selective precharge has been combined with positive feedback in the charging unit of CR type MLSA. After observing some characteristics of IP addresses, the ML has been partitioned into two segments to implement selective precharge. The first segment charging unit has been designed with positive feedback to speed-up match detection in that segment and to reduce energy consumption. The second segment charging unit has been designed with low resistance charging path for fast charging of the segment. We have also eliminated the need for additional control signals other than the reset and start signals.

The rest of the paper is organized as follows. Section III presents the background, circuit implementation and operation of the proposed ML sensing scheme. Section IV presents simulation results and comparison of the proposed scheme with the CR, MD and AF sensing schemes. Also, simulation results considering process variations in our scheme are presented in this section. Section V includes conclusions and extension of the implementation.

III. RESISTIVE FEEDBACK WITH ML SEGMENTATION SCHEME

A. Background

In internet protocol version 4 (IPv4) IP address length is 32 bit. But not all the IP addresses are always 32 bit long. Often address lengths are smaller and the corresponding entries (also called prefix) in the routing table are filled with don't care values in less significant bits. The longest prefix match requires the entries to be sorted in the table according to the number of don't care values in each entry. So, the most significant bits (MSBs) are not don't care bits. In general most significant 8 bits are never don't care [16]. According to the simulation result in [17], around 98% of the mismatched MLs can be identified by comparing most significant 8 bits. Keeping this in mind, we propose a ML segmentation scheme where the ML has been divided into two segments – first segment containing 8 TCAM cells and the second one containing the rest (24 TCAM cells). Initially search will be performed in the first segment using 8 MSB bits of search data. Only if the first segment is fully matched the second segment will be activated and compared with remaining bits of the search data. It should be noted here that one 'bit' in TCAM is actually coded two binary digits as mentioned in section I. Like the original CR

scheme a dummy ML (DML), segmented like a regular ML, has been used to control the charging durations of the segments. The new internet protocol version 6 (IPv6) addresses are 128 bit long and the corresponding forwarding table requires a large TCAM array. In this paper we consider forwarding table containing smaller IPv4 addresses to keep simulation time within reasonable limit. But of course the same concept can be extended to IPv6 forwarding table as discussed in section V.

In addition to proposing active feedback MLSA, [15] introduced the concept of feedback with resistive shielding using an nMOS transistor in the charging unit of non-segmented ML. The transistor was operated in resistive region by a constant gate voltage. We modified that design by using an nMOS transistor with variable gate voltage and adjusting the gate dimensions of this transistor and the charging pMOS transistor in the first ML segment charging path. The nMOS transistor in our scheme operates in saturation region and its varying channel resistance (which varies with V_{gs}, V_{ds} and V_t) acts as the feedback element only in the first segment MLSA. This modification results in less routing complexity and elimination of one extra analog voltage signal at the gate.

B. Circuit Implementation and Operation

Fig. 3 shows a TCAM word and a dummy word of the proposed scheme. At first MLRST resets the voltages of all ML segments, sensing nodes (SNs) and ML segment outputs (MLSO1, MLSO2, DMLSO1, DMLSO2) to ground. The search data is applied to the SLs. Then MLEN initiates the search operation. It starts charging the first segments of all MLs and the DML by turning on P1. Initially first segments of both matched and mismatched MLs get the same current through P1. As the ML voltage goes up the feedback action of nMOS N1 begins. With increasing ML voltage V_{ds}, V_{gs} of N1 decrease and V_{sb} increases causing threshold voltage to rise. So, the channel resistance increases. More current is diverted to the sensing node capacitance (C_{SN}). Since C_{SN} is small, it can be charged very quickly. Matched ML segments are disconnected from ground and hence they charge much faster than the mismatched ML segments. This makes C_{SN} of a matched ML segment charge much quicker than C_{SN} of a mismatched ML segment. As soon as the SN voltage in a matched segment exceeds the sensing threshold voltage (V_t of N2) of the sensing unit, MLSO1 is pulled to high. DML segment 1 works exactly like a matched ML segment 1. A high DMLSO1 stops flow of charging current to the ML (and DML) first segments by turning off P1 and initiates the charging of the second DML segment by turning on P2. The SN voltages of mismatched segments do not get sufficient time to charge up to the sensing threshold of the corresponding sensing units. So, outputs of only fully matched ML first segments are high.

For fully matched ML first segments the MLSO1 signals turn on transistors P2 and charging of second
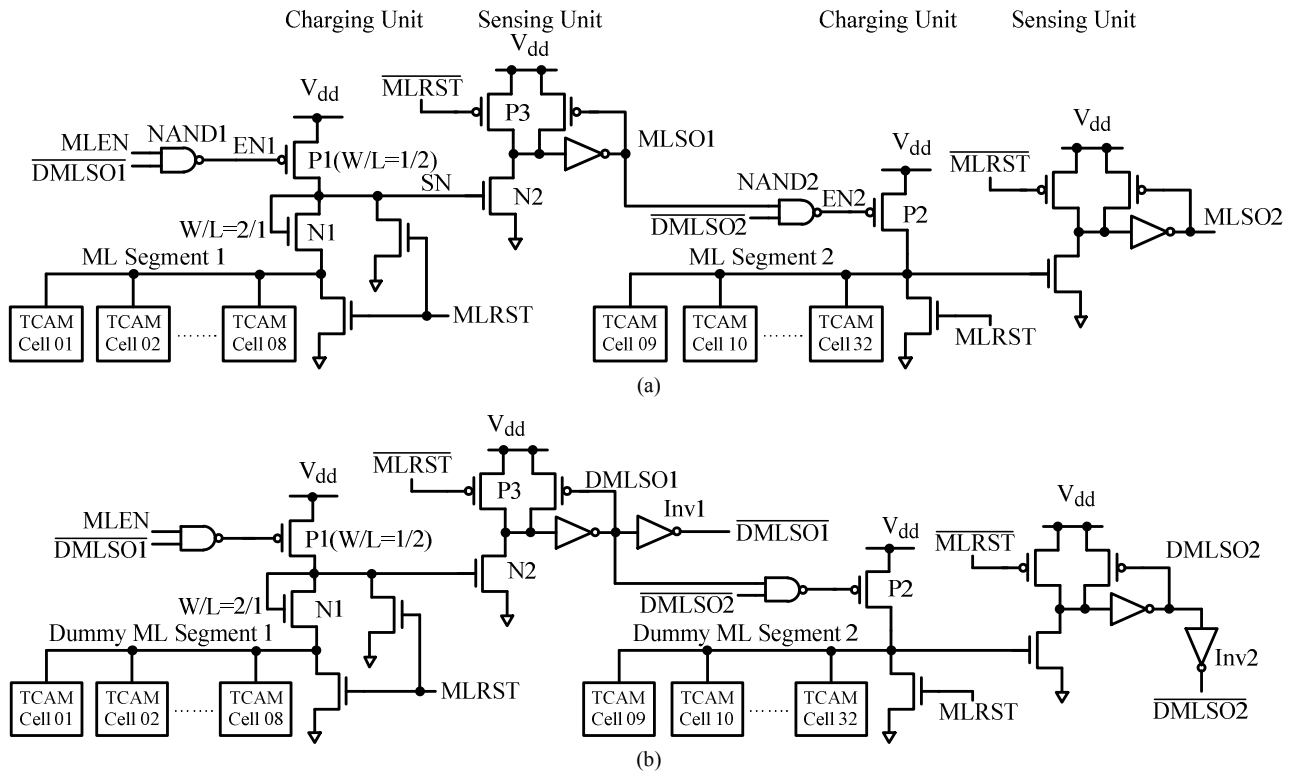
Figure 3. Mixed circuit, symbol and block diagram of the proposed ML sensing scheme - (a) one TCAM word and (b) a dummy word resembling an always-matched word.

segments starts. No feedback transistors have been used in the MLSAs here since only a few second segments are expected to be activated. As soon as the ML voltage of the matched second segment exceeds the sensing threshold of the sensing unit, MLSO2 is pulled to high and further charging is terminated by DMLSO2 by turning off P2. Voltages of mismatched second segments cannot reach the sensing threshold by that time. Thus, final match decision is obtained at MLSO2.

In the original CR scheme an adjustable delay (Δ in Fig. 2b) was used after DML output to delay the termination of ML charging to ensure proper match detection. We find that in our scheme the delays introduced by the series inverters (Inv1 and Inv2) and the NAND gates (NAND1 and NAND2) are sufficient to serve that purpose even under the worst case process variation. So, we have not used any delay element.

The gate dimensions of the transistors in the charging unit of the first segment (P1 and N1) have to be chosen carefully. If the initial charging current (before feedback starts) is high and the channel resistance of the feedback nMOS is too large then C_{SN} charges so quickly that correct detection of mismatch in the first segment becomes impossible. Initial current has been reduced by increasing gate length of P1 and channel resistance of N1 has been reduced by increasing gate width of N1.

IV. SIMULATION RESULTS AND COMPARISON

In our initial work [18] we simulated one 32 bit TCAM word and a dummy word in both CR and our proposed scheme and provided some preliminary analyses of those

schemes. As mentioned before, TCAM actually works in the form of array i.e. multiple words × multiple bits. In this paper we have used 130nm 1.2V CMOS logic to simulate 64-words×32-bits TCAM arrays. So, different capacitive effects are simulated more accurately. Predictive technology model (PTM) [19] has been used in HSPICE for the simulation. Comprehensive simulations of proposed, CR [13], MD [14] and AF [15] schemes have been performed to analyze and compare various aspects of the schemes. The popular CR scheme has been used as the reference design as [14], [15] and this work focus on enhancing the performance of the original CR scheme. For the sake of fair comparison no additional delay has been used after DML in CR MLSA (Δ=0 in Fig. 2b) as that would increase the energy consumption of CR scheme. The CR scheme functions correctly with this setting in ideal case i.e. without consideration of any process variation and noise. Moreover, different control voltages in CR, MD and AF schemes have been set to values which will yield maximum search speed for all the schemes.

A. Voltage Margin

Among all types of mismatches 1-bit mismatch causes maximum resistance in the ML pull-down path since there is only one path through two nMOS transistors. If there are multiple mismatches, multiple pull-down paths exist in parallel and hence the equivalent resistance of ML to ground path is lower. Maximum resistance in the pull-down path means less charge leakage from ML to ground during match evaluation. Hence ML with 1-bit mismatch charges faster than MLs with more than one

mismatch. So, 1-bit mismatch is the hardest to detect and it has the highest probability to be detected as a false match. So, we compare voltage wave shapes of MLs and SNs with full match and with 1-bit mismatch.

Fig. 4 shows the variations of voltages of ML and SN for a fully matched first segment and for a 1-bit mismatch in the same segment of the proposed scheme. ML power consumption is directly proportional to the ML voltage swing [2]. The maximum voltage to which a matched ML first segment needs to be charged for correct match detection is only 554mV (46% of V_{dd}). In CR, MD, and AF schemes the corresponding values are 1019mV, 1012mV and 1017mV respectively. Also, for different number of mismatches in the first segment of our scheme the voltage swings are lower. Most of the mismatches are supposed to be detected in the first segment comparison. So, the reduced ML voltage swings in the first segment will definitely result in huge energy saving. The other three schemes (CR, MD, AF) do not use ML segmentation. So, these techniques need to charge the full ML capacitance (C_{ML}) of all words during the search. In the proposed technique the capacitance needs to be charged in the first segment is much lower than C_{ML} (roughly $C_{ML}/4$ if we ignore C_{SN}). In spite of having lower capacitance, ML segment is charged to a lower voltage because of feedback. Though some energy is consumed in charging C_{SN} but this energy is small as C_{SN} is small. Also, it is clear from Fig. 4b that from initiation
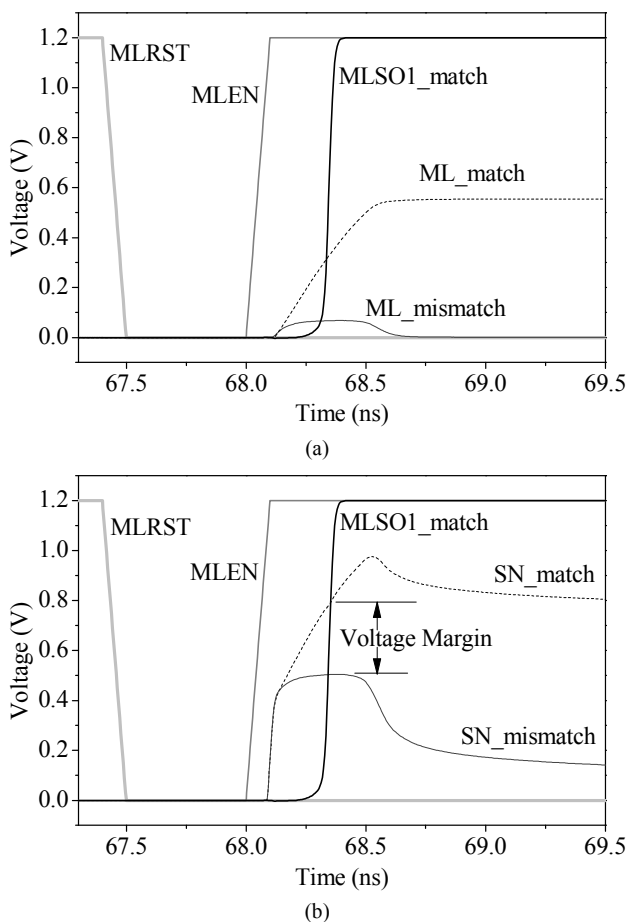
of charging up to ~125ps, C_{SN} of both matched and mismatched segments charge at the same rate due to same initial currents supplied by the charging pMOS P1. After that the feedback action begins causing C_{SN} of matched segment to charge at higher rate than that of mismatched segment.

Fig. 5 shows the variation of ML voltages for a full match and for a 1-bit mismatch in the second segment when first segment is fully matched. Due to simpler charging unit the ML voltage magnitudes are higher than those in first segment or those in other schemes. But, since only a few second segments will be activated in a search, the additional energy consumption arising from second segment charging will not be significant.

The SN and ML voltage magnitudes shown in Fig. 4 and Fig. 5 are higher than those found in [18]. This is expected because here we have simulated the whole TCAM array instead of only one word as was simulated in [18]. So, higher capacitances are seen by different internal signals and charging of segments goes on for longer time. This also causes slight increase in search time compared to [18] as will be shown later.

Voltage margin is defined as the difference between the sensing threshold of the sensing unit and the maximum voltage to which a 1-bit mismatched ML (SN for first segment) is charged. It has been calculated using graphical method shown in [13]. Fig. 4(b) and Fig. 5 show the voltage margins for first and second segment of our scheme, respectively. Higher is the voltage margin greater is the capability of the circuit to handle process variation. Table I shows the comparison of voltage margins in different techniques.

Small value of C_{SN} is the reason for smaller voltage margin in the first segment. Voltage margin in the second segment is also lower than that in other schemes. These reduced voltage margins are still sufficient to take care of the process variations as will be shown later.

Figure 4. Variations of (a) ML and (b) SN voltages with match and 1-bit mismatch in the first segments of the proposed scheme.
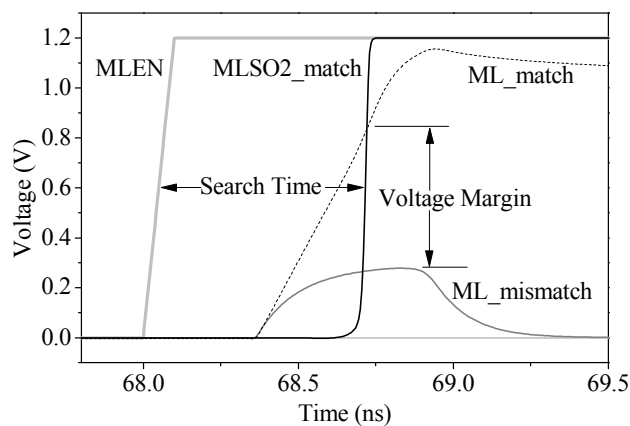

Figure 5. Variations of ML voltages with match and 1-bit mismatch in the second segments of the proposed scheme.

TABLE I.
VOLTAGE MARGIN COMPARISON OF THE PROPOSED, CR, MD AND AF SCHEMES

Proposed Scheme		CR Scheme	MD Scheme	AF Scheme
Segment 1	Segment 2			
289mV	568mV	619mV	618mV	623mV

B. Charging Currents

We have simulated the variations of C_{SN} charging currents for matched and mismatched ML first segments in our scheme. Fig. 6 shows the simulation results. Initially, for both matched and mismatched MLs, the charging currents are same. After about 125ps the feedback action begins. Matched ML causes more current to be channeled to SN while the charging currents for mismatched MLs decrease with increasing number of mismatches. After the ML charging current is shut off at the end of search phase the charge stored in C_{SN} passes to ML through the feedback transistor N1 as N1 is still working in saturation mode. That is why, SN voltage keeps decreasing (Fig. 4b) and SN current becomes negative (Fig. 6) after MLSO1 goes high. This reduction of SN voltage may turn off N2 in case of a full match. The inverter of sensing unit can maintain a high output even at this condition. Simulation shows that off-current through the resetting pMOS (P3 in Fig. 3) in the sensing unit can flip the MLSA output in match case if circuit remains idle for a long time (~1μs). But with hundreds of millions searches per second performed in modern routers that will never happen. The magnitudes of charging currents are small signifying that charging of C_{SN} does not consume much energy.

We have also simulated the transient charging currents of ML segment 2 for matched and mismatched cases which are plotted in Fig. 7. The charging unit is simpler and has lower resistance in the charging path compared to other techniques. That is why the magnitudes of currents are large. These large currents will not contribute significantly to the total energy consumption as number of activated second segments will be small. But definitely these will increase the peak dynamic power consumption as will be shown later. As expected, the charging current in case of full match decreases gradually as the ML segment voltage rises rapidly (Fig. 5). In case of mismatches there are fixed resistance paths from ML to ground and hence currents remain almost constant in mismatched MLs during the whole charging time. 2-bit mismatch offers lower resistance path than 1-bit mismatch and hence current in 2-bit mismatch case is higher than that in 1-bit mismatch case. This is the reason that energy consumption per word per search increases
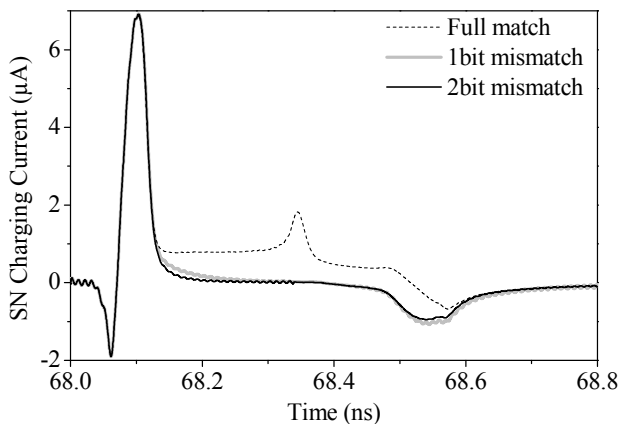

Figure 6. Variations of charging currents of SN with number of mismatches in the first segments.
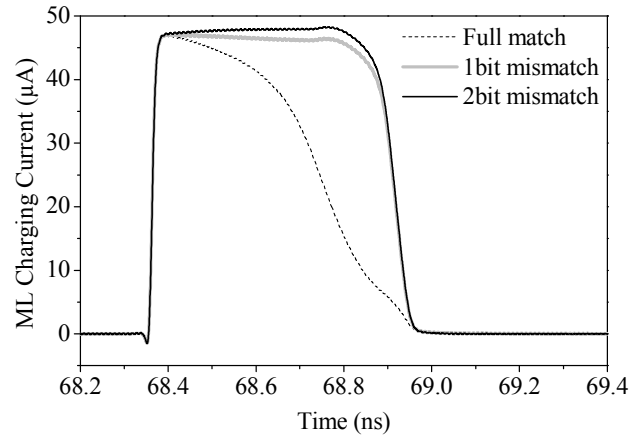

Figure 7. Variations of charging currents of ML with number of mismatches in the second segments.

with number of mismatches in the second segment as was found in [18].

C. Search Time

Search time is defined as the time from 50% (0.6V) of MLEN to 50% (0.6V) of the final output of a matched ML (Fig. 5). Table II shows the comparison of search times of different schemes. It also shows percentage reduction (negative) or increase (positive) in search time with respect to CR scheme.

Neither [14] nor [15] presented any speed comparison with the CR scheme. According to our simulation results, our scheme offers much higher search speed than any other schemes even with the maximum speed settings for all. This speed improvement is attributed to – *i)* fast match detection in the first segment as less amount of capacitance ($C_{ML}/4$) needs to be charged to lower voltage (46% of V_{dd}) and *ii)* quick ML charging in the second segment because of higher charging current supplied by the charging unit. Faster match detection will in turn shut off the ML charging currents earlier resulting in reduced energy consumption.

The search times obtained in this work is greater than those obtained in [18] (600ps in our scheme and 810ps in CR scheme) because of the reason stated earlier.

D. Energy Consumption

Both [14] and [15] reported reduction of average ML sensing energy in unit of fJ/bit/search compared to CR scheme. Reference [14] reported an energy reduction of 40% using 130nm CMOS simulation while [15] reported 56% energy reduction using 180nm CMOS measurement. It was shown in [14], [15] and [18] that the energy consumption per word (or per bit) per search changes with mismatch conditions i.e. full match, 1-bit mismatch,

TABLE II.
SEARCH TIME COMPARISON OF THE PROPOSED, CR, MD AND AF SCHEMES

	Proposed Scheme	CR Scheme	MD Scheme	AF Scheme
Search time (ps)	627	853	864	869
% change w.r.t. CR	-26.5%	0	+1.3%	+1.9%

2-bit mismatch etc. The average energy consumption can be calculated from the probabilities of different types of mismatch conditions and energy consumed for each type of condition. In case of IPv6, with many still unallocated IP addresses and many used IP addresses being less than the maximum length [20] the distribution of IP addresses is never even. So, assessing probabilities of different mismatch conditions may be difficult. So, we prefer a different approach for energy comparison. We have emphasized on the lower boundary (worst case) of energy saving in our scheme.

Fully matched words consume the highest energy among all types of words. In case of mismatched words we showed in [18] that energy per word decreases with number of mismatches in the first segment while in second segment this increases with number of mismatches. So, 1-bit mismatch will cause maximum energy consumption per word if the mismatch is detected in the first segment and minimum energy consumption per word if the mismatch is detected in the second segment. In the second segment, portions of most of the words contain don't care values as mentioned in section III. So, probability of having large number of mismatches in a word is low in this segment. Therefore, we assume that on average number of mismatches in the activated second segments will be 4 per word. Moreover, number of full matches in the array is generally small. Based on this, we construct a routing table which will cause maximum energy consumption in our scheme. In this routing table there are 4 fully matched words, 54 words with 1-bit mismatch in the first segment and 6 words with 4-bit mismatch in the second segment. Instead of assuming 98% mismatch detection in the first segment [17] we assumed a pessimistic 90% mismatch detection (90% of 60 mismatched words) in that segment. This pessimistic assumption will further increase the energy consumption since more mismatch detection in the second segment means more energy consumption [18]. We simulated our scheme and CR scheme using this routing table and calculated the total energy consumption by the TCAM arrays from the dynamic power consumption curves. Table III shows the calculated and reported energy savings.

Reference [14] and [15] reported average and maximum energy savings, respectively. So, for the sake of fair comparison we have also calculated the maximum and average energy saving in our scheme without using any probability based approach. In order to calculate maximum energy saving (minimum energy consumption) in our scheme we simulated our scheme and CR scheme with a routing table containing 1 fully matched word, 62 words (98% of 63 mismatched words) with 8-bit mismatch in the first segment and 1 word with 1-bit mismatch in the second segment. The average saving has

been calculated from the minimum and maximum savings. In [18], based on the one word simulations, we calculated 47% energy reduction possibility in our scheme. The result was an overestimation since capacitive effects were less accurately simulated.

E. Peak Dynamic Power

Peak power consumption with worst case data pattern is a critical CAM performance criterion [2]. Many energy saving techniques concentrate on reducing average power consumption but the peak power consumption increases. Increased peak power consumption means more power has to be allocated for the TCAM chip which will be useful only for a short duration but during rest of the search cycle most of that allocated power remains unutilized. So, lower peak power consumption means cheaper supply can be used or the extra power can be used for other components. The worst case routing table used in energy comparison has been used to obtain peak power consumptions of various schemes. Table IV shows the comparison.

In terms of peak power consumption our scheme is better than MD and AF schemes. Compared to CR scheme the peak power consumption in our scheme is 36% higher. This peak power consumption occurs during the second segment comparison in our scheme due to large second segment charging currents. If the charging currents can be limited the peak power consumption can be reduced. This can be done in two ways –

i) The channel resistance of the charging pMOS P2 can be increased. But this drastically affects the search time. Doubling the channel length reduces peak power consumption to 3173μW while search time is increased to 1332ps.

ii) Same feedback technique as in MLSA of segment 1 can be used in MLSA of segment 2. This results in a peak power consumption of 3368μW and search time of 760ps.

So, reduction of peak power consumption can be achieved at the expense of reduced search speed and increased circuit area.

F. Transistor Count

Table V shows the number of extra transistors per

TABLE III.
COMPARISON OF ENERGY SAVINGS COMPARED TO CR SCHEME

Proposed Scheme	MD Scheme	AF Scheme
31% (minimum) 39% (average) 47% (maximum)	40% (average)[14]	56% (maximum)[15]

TABLE IV.
COMPARISON OF PEAK POWER CONSUMPTIONS BY 64 WORD × 32 BIT TCAM ARRAYS IN DIFFERENT SCHEMES

	Proposed Scheme	CR Scheme	MD Scheme	AF Scheme
Peak power (μW)	3691	2709	4641	4319
% change w.r.t. CR	+36%	0	+71%	+59%

TABLE V.
COMPARISON OF EXTRA TRANSISTOR COUNT AND PERCENTAGE INCREASE IN DIFFERENT SCHEMES COMPARED TO CR SCHEME

	Proposed Scheme	MD Scheme	AF Scheme
Number of extra transistors	12	5	3
% increase w.r.t. CR	2.3%	0.95%	0.57%

word required by different schemes and percentage increase in transistor count with respect to CR scheme. We implemented TCAM cells in all schemes using popular 6T SRAM cells though the original CR scheme [13] used 4T asymmetric cells. Compared to CR scheme the percentage increase in transistor count in our scheme is small.

G. Worst Case Process Variation

Positive feedback systems are sensitive to process variations [14], [15]. So, we perform simulations to determine the robustness of our scheme to worst case process variations. We include both the segments (segment 1 with feedback and segment 2 without feedback) in the simulations. Two problem scenarios can arise.

The first scenario is SN and ML voltages in 1-bit mismatched ML segments may rise faster than typical values and may trigger the sensing units to produce wrong match decision before the charging pMOS transistors are turned off by a typical DML. In order to identify what factors can increase the voltages in both the segments we reproduce the circuit with SN and ML charging and discharging paths in case of a 1-bit mismatch in Fig. 8.

In segment 1 of Fig. 8a the SN voltage will rise faster than the typical if

- larger charging current is supplied by M1. This can happen if the width of M1 (W_{M1}) increases due to process variation,
- transistor M2 offers greater resistance due to reduction in gate width (W_{M2}) causing greater portion of total charging current to be diverted to SN and
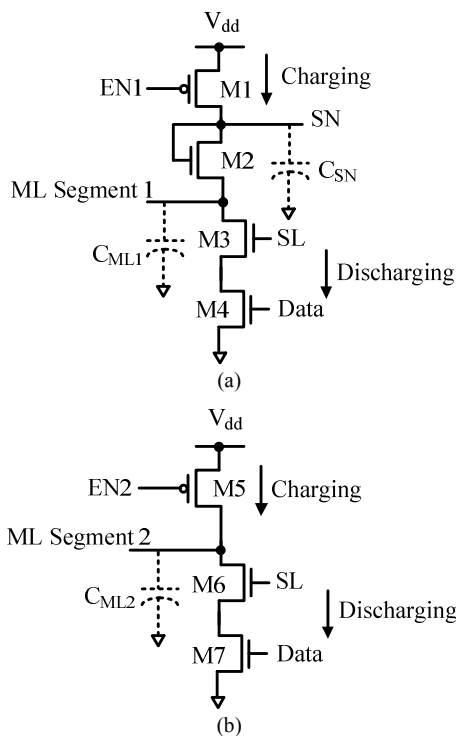

Figure 8. Circuit diagrams of (a) segment 1 with 1-bit mismatch and (b) segment 2 with 1-bit mismatch.

- ML segment 1 capacitance (C_{ML1}) charges faster than the typical case causing C_{SN} to be charged faster also. This can happen due to reduction in gate widths (W_{M3}, W_{M4}) and increase in threshold voltages (V_{tM3}, V_{tM4}) of M3 and M4 causing less charge leakage from C_{ML1} to ground.

In segment 2 of Fig. 8b the ML voltage will rise faster if

- transistor M5 supplies greater charging current due to increase in its width (W_{M5}) and
- transistors M6 and M7 have reduced gate widths (W_{M6}, W_{M7}) and increased threshold voltages (V_{tM6}, V_{tM7}) as M3 and M4 in segment 1.

All of the above scenarios have been incorporated by

- increasing W_{M1} by 20%, decreasing W_{M2}, W_{M3} and W_{M4} by 20% and increasing both V_{tM3} and V_{tM4} by 20% in only one word having 1-bit mismatch in the first segment,
- increasing W_{M5} by 20%, decreasing W_{M6} and W_{M7} by 20% and increasing both V_{tM6} and V_{tM7} by 20% in only one word having 1-bit mismatch in the second segment and
- keeping all other 62 words and the dummy word in the TCAM array typical (no process variation).

Fig. 9 shows the first segment SN charging currents and transient voltages in both the process varied and typical words. The SN charging current in process varied (PV) segment is initially higher than that of typical segment with match and 1-bit mismatch. But with passage of time the charging current in PV segment falls below the charging current in typical matched segment. Higher initial current in PV segment causes higher SN voltage than that in typical mismatched segment resulting in reduction of voltage margin from typical value of 289mV to 204mV. This margin is still sufficient to take care of significant threshold voltage shift of sensing nMOS (N2 in Fig. 3) due to process variation.

Fig. 10 shows the ML charging currents and voltages in the process varied and typical second segments. The ML charging current in process varied (PV) segment remains higher than those of typical segments with match and 1-bit mismatch during the whole charging period. Higher charging current in PV segment causes higher ML voltage than that in typical mismatched segment resulting in reduction of voltage margin from typical value of 568mV to 280mV.

The second problem scenario is when only dummy word goes through process variations such that its ML segments and SN charge faster than a typical fully matched word. The dummy word segments will turns off the charging pMOS transistors earlier since its voltages will reach sensing threshold of sensing units earlier. A typical matched word may not be able to trigger its sensing units by that time and may fail to be detected correctly. Since a dummy word is always matched, transistors M3, M4, M6 and M7 shown in Fig. 8 remain off for a DML and it does not matter whether these transistors go through process variations or not. So, this scenario is simulated by assuming only DML goes through process variations with 20% increase in W_{M1},
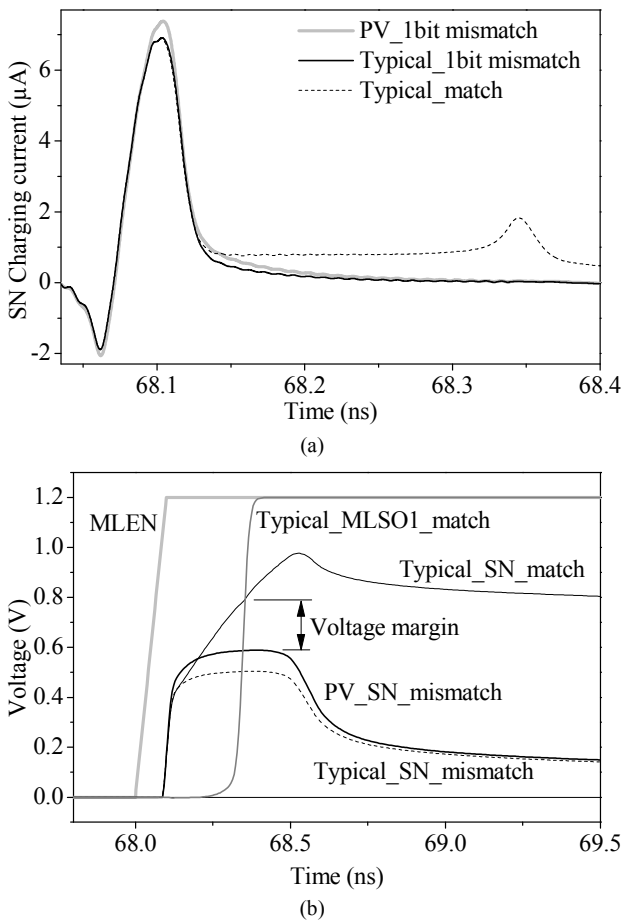
Figure 9. Variations of (a) SN charging currents and (b) SN voltages with typical match, typical 1-bit mismatch and process varied (PV) 1-bit mismatch in the first segments.
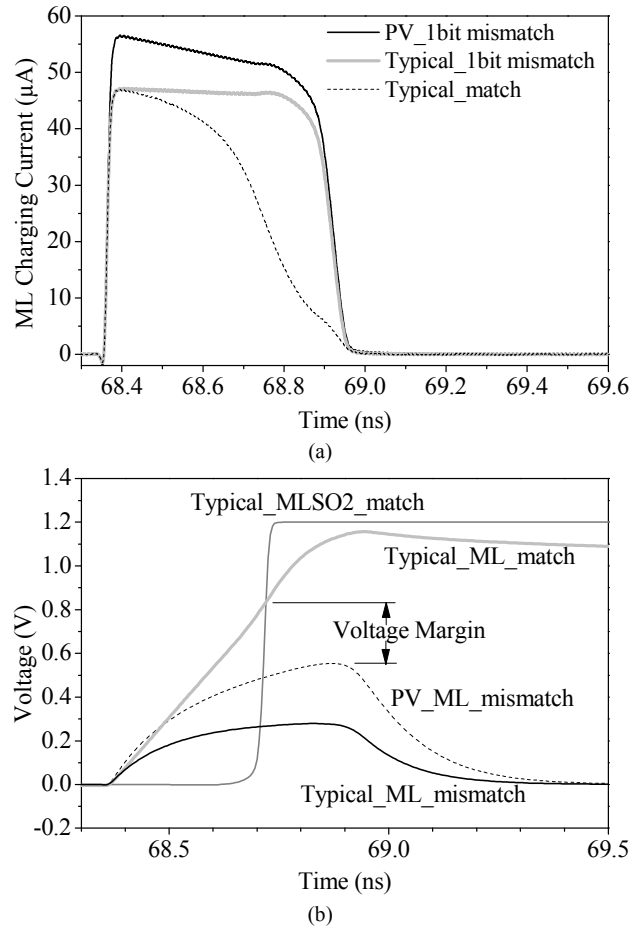

Figure 10. Variations of (a) ML charging currents and (b) ML voltages with typical match, typical 1-bit mismatch and process varied (PV) 1-bit mismatch in the second segments.

W_{M5} and 20% reduction in W_{M2}. All other words in the array remain typical.

Fig. 11 shows the SN voltages and segment outputs of the process varied DML first segment and typical matched first segment. As expected, C_{SN} of DML charges faster and to a higher voltage than that of a typical C_{SN}. So, DMLSO1 becomes high before a typical MLSO1. This is exactly the opposite of what happens in case of a typical DML. A typical MLSO1 can become high in spite of earlier transition of DMLSO1 because the transition of DMLSO1 is sensed by P1 (Fig. 3a) after a finite delay caused by the series inverter Inv1 (Fig. 3b) and the gate NAND1 (Fig. 3a).

Fig. 12 shows the ML voltages and segment outputs of the process varied DML second segment and typical matched second segment. As expected, second segment capacitance (C_{ML2}) of DML charges faster and to a higher voltage than a typical C_{ML2} in matched segment 2. So, DMLSO2 becomes high earlier than typical matched MLSO2. Here again a typical MLSO2 can become high in spite of earlier transition of DMLSO2 because of the delay introduced by the inverter Inv2 (Fig. 3b) and the gate NAND2 (Fig. 3a).

V. CONCLUSIONS

We presented a ML sensing scheme for TCAM using ML segmentation and positive feedback in the MLSA of the first segment. The objective of the scheme was to achieve both high speed and low energy consumption. Simulation of 64-word×32-bit TCAM array shows at least 31% energy saving compared to conventional CR scheme. Feedback in the first segment charging unit and lower resistance in the charging path of the second segment charging unit achieve 26.5% speed enhancement. In contrast to many schemes available in literature we tried to keep the implementation complexity low by eliminating the need for any analog control voltage. It was shown that no scheme can offer performance enhancement in terms of all the parameters. A trade-off has to be maintained between voltage margin, search speed, energy consumption, peak power consumption, area and implementation complexity. Our scheme offers a well balanced solution while providing excellent enhancement to important performance parameters i.e. search speed and energy consumption.
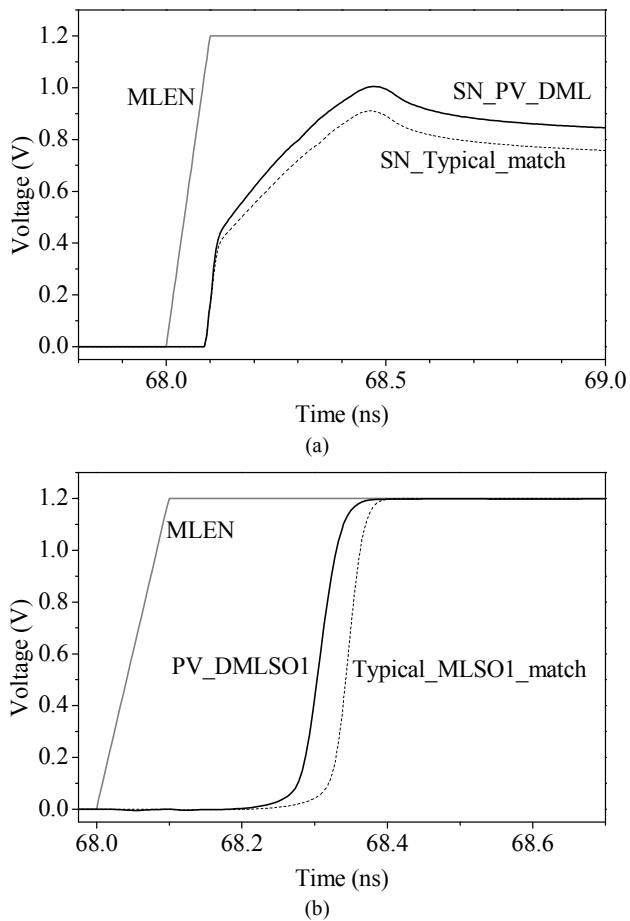
Figure 11. Variations of (a) SN voltages and (b) segment output voltages with typical matched ML and process varied (PV) DML first segments.
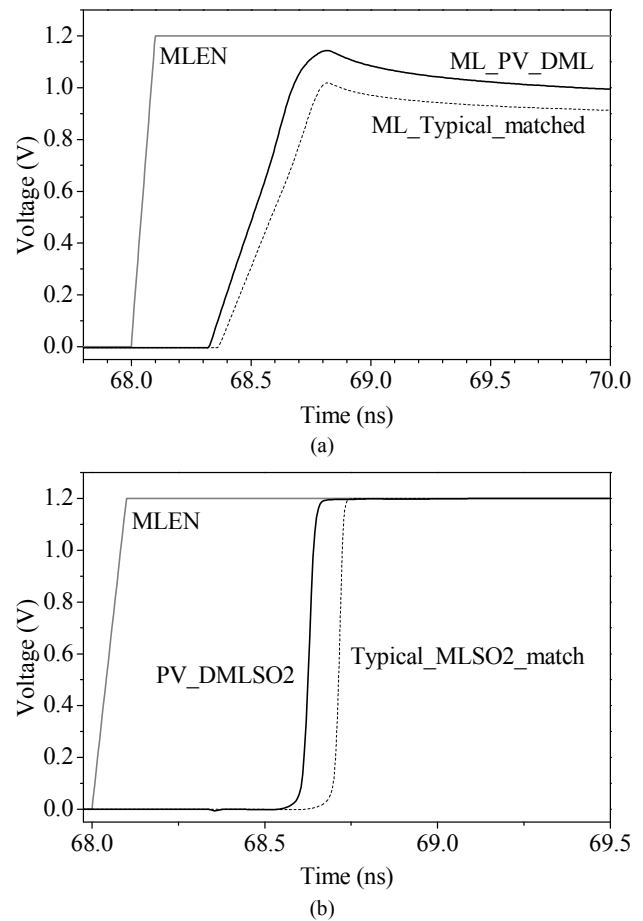

Figure 12. Variations of (a) ML segment voltages and (b) segment output voltages with typical matched ML and process varied (PV) DML second segments.

TCAM continues to be a popular choice in IP packet forwarding and classification applications which use newer IPv6 addresses. Our technique can be used in such applications with minor modification. After studying over 3850 prefixes from six IPv6 routing tables taken from different countries, it was reported in [20] that the second 16 bits (17th to 32nd) of the IPv6 addresses rarely match. The routing tables studied by [20] had at most 15 prefixes (0.39%) with the same value in the second 16 bits i.e. the maximum match probability in the second 16 bits was found to be 0.39%. So, the minimum mismatch probability in the second 16 bits can be as high as 99.61%. This mismatch probability is even better than the 98% mismatch probability in the first 8 bits of IPv4 addresses mentioned in section III. So, the same concept of selective precharge can be applied to IPv6 addresses too. The second 16 bits (17th to 32nd) can be used to construct the first segment (TCAM cell 17 to TCAM cell 32 for ML segment 1 in Fig. 3) and second segment can be constructed with the rest of the bits (1st to 16th and 33rd to 128th TCAM cells in ML segment 2 of Fig. 3). This will result in excellent filtering of the mismatched words (more than or equal to 99.61%) during the first segment comparison and hence smaller percentage of second segment activation than IPv4 case. Mismatch detection in second segment comparison requires more energy per bit per search than mismatch detection in the

first segment comparison as activation of second segment requires additional energy. So, less percentage of second segment activation in IPv6 should result in greater percentage of energy saving than the IPv4 case.

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